

Ken Takenuchi et al. -- U.S. Serial No. 10/073,999**REMARKS**

The Office Action of January 8, 2003 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested.

Claims 47-67 remain in this application.

Claims 47-50 and 55-57 have been amended. Support for these amendments may be found at least in Figure 9, starting at page 30 of the specification. Other Figures also support the new amendments to the claims.

The claims stand rejected under 35 USC 102(a) over Hemink et al. Applicants traverse.

Claim 47, for example, has been amended to read as follows:

“ a data circuit connected to one ends of said first and second signal lines, and including a capacitor and a latch circuit;
wherein first program / read data of said first memory cell is temporarily stored in said data circuit, and second program / read data of said second memory cell is held by said second signal line.”

Hemink fails to disclose the data circuit as claimed as including the capacitor and latch circuit. While Hemink shows a capacitor C1, the combination of the capacitor and the bit line controller 103 of Figures 13 and 16 does not disclose the system of claim 47.

Claims 48-50 and 55-57 have been similarly amended with respect to the latch circuit and capacitor and are similarly allowable over Hemink.

It is believed that no fee is required for this submission. If any fees are required or if an

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overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733 accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same.

Respectfully Submitted,

By:


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